Integrated Frequency Counter for Multidimensional Seismometric System

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We present an integrated frequency counter developed for a multidimensional seismometric system. The aim of the counter is to accurately measure 600 MHz signal from laser gyroscopes and distinguish small frequency changes related to vibrations of the ground surface. The design is implemented in a Kintex-7 field programmable gate array (FPGA) device manufactured by *AMD Xilinx*. Four parallel measurement channels are designed that combine timestamping and interpolation methods. According to test results the counter is able to measure signals of up to 1 GHz frequency without prescaling and with 9 significant digits in a 1 ms time gate.

Keywords—FPGA, frequency counter, linear regression, seismometric system;

I. INTRODUCTION

Seismological studies focus on the study of Earth movements, which include earthquakes and other events that generate seismic waves [1, 2]. The earthquake can be fully described by determining the displacement along three perpendicular axes *x, y, z* as well as measuring the rotational speed ωx , ωy , ωz around the *x, y* and *z* axis. During many years of seismic observations, despite of low amplitude, it turned out that rotational vibrations have a significant impact on the buildings of large linear dimensions. Due to the technological possibilities, the measurement of rotational waves was possible at the beginning of the 21st century with high sensitive gyroscopes. The development of precise time sources and the dissemination of the optical gyroscope technology could record and analyze rotational vibrations. The angular velocities of the above vibrations are measured in [mrad/s] and parts thereof. Therefore, gyroscopes must be highly sensitive. Optical gyroscopes use the Sagnac effect and, due to their construction, can be divided into two groups:

- Laser Gyro (LG) - directing the laser beam is carried out by using a set of mirrors;
- Fiber Optical Gyro (FOG) - directing the laser beam is carried out by using optical fibers.

The sensitivity of the designed seismometric system [3] largely depends on the accuracy of the frequency evaluation of signals obtained from LGs. The classical reciprocal frequency counter simultaneously counts full periods of the measured signal during selected time gate and accurately determines the duration of that gate by a time interval counter. In the so called Π counter only the beginning and end of the gate is sampled. Higher accuracy can be obtained with faster sampling and statistics (Λ and Ω counters) [4]. Among the mentioned types of meters Ω counters most accurately evaluate the average value of the frequency but at the cost of greater computational complexity (they involve linear regression).

In this work we present a dedicated integrated Ω counter that can measure relatively high frequencies without prescaling (tested up to 1 GHz), and which allows for accurate timestamping of obtained results. These properties are crucial for the newly developed multidimensional seismometric system.

II. INTEGRATED FREQUENCY COUNTER DESIGN

In the multidimensional seismometric system it is assumed that the measured frequency should be around 600 MHz and be measured every 1 ms simultaneously in 3 channels. Additionally, one extra channel is implemented to register One Pulse Per Second (1PPS) signal from Global Navigation Satelite System (GNSS) to enable high accuracy timestamping of obtained results.

Figure 1 presents a block diagram of the designed frequency counter. The counter contains 4 measurement channels. One common gate generator is used for all channels, which sets the pace for collecting timestamps in each of them. The gate generator is programmable in a range from 40 ns up to 1 s. The measurement channel can be divided into 5 parts: (1) an input circuit with double synchronizer, (2) an event counter and register, (3) a main clock counter and register, (4) a time-to-digital converter (TDC) and code processor, and (5) a memory.

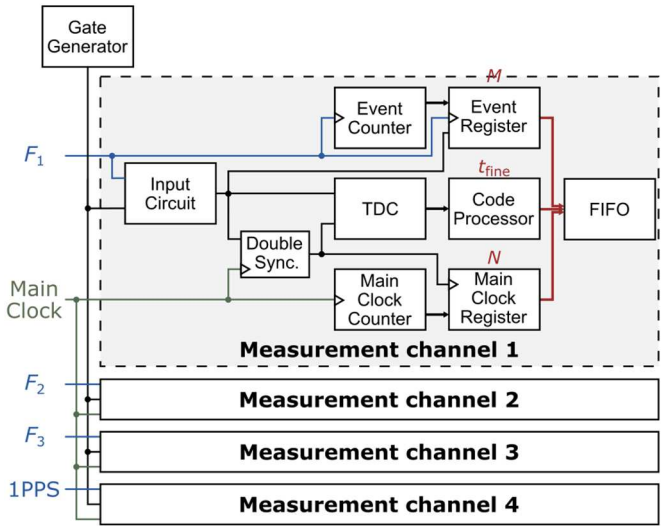

Fig. 1. Block diagram of an integrated frequency counter.

Two binary counters counts numbers of both clock and input signals periods. Occurrence of an input event (signal edge) causes the state of both counters to be stored in the main clock (N) and event (M) registers, respectively. The task of the input circuit is to register the nearest edge of the input signal (F) after the occurrence of the active state of the gating signal. The registered edge is then used as a start signal in the TDC and disables the event register. The registered signal is also synchronized to the main clock signal and then used as a stop signal in the TDC and as a latching signal in the main clock register. The TDC accurately quantizes time intervals between input signal edge and the next main clock signal. To achieve picosecond resolution we have merged 4 time coding lines, a combination of a tapped delay line and a register, as a single TDC in each channel [5].

The result from the TDC is processed in the embedded code processor. The code processor calculates the TDC's transfer characteristic during calibration phase, and then, during measurement phase, calculates the measurement result (T_{fine}) based on it. The calibration phase involves taking a series of multiple measurements of time slices of random duration (the statistical code density test [6]). On this basis, it is possible to accurately determine the size of individual quantization steps and thus, improve the precision of measurement. Data obtained from the registers and TDC (N, M, T_{fine}) is then stored in a First-In-First-Out (FIFO) memory as a timestamp.

Using the classic reciprocal method (Π counter), the frequency can be calculated based on two registered neighboring timestamps (TS) from a given channel $TS_1(N_1, M_1, T_{\text{fine1}})$ and $TS_2(N_2, M_2, T_{\text{fine2}})$, and the formula:

$$f_{\Pi} = \frac{M_2 - M_1}{t_2 - t_1}, \tag{1}$$

where T_{clk} is the main clock signal period (1/710 MHz≈1.4 ns) and t represents time of the event occurrence calculated using equation (2).

$$t = N \times T_{clk} + t_{fine}, \tag{2}$$

A more accurate average value of the frequency can be determined in Ω counter by finding the coefficient of a line describing the relationship between the number of periods of the measured signal (M) and successive time values (t). The best fit of the line to the measurement series is provided in this case by the least squares method:

$$f_{\Omega} = \frac{n\sum M^2 - (\sum M)^2}{n\sum t \times M - \sum t \times \sum M}, \tag{3}$$

where n is a number of timestamps registered in the range of the measuring gate.

Determining the frequency from (3) typically requires operating on large numbers, represented in the digital system by multi-bit vectors. In our first approach, the timestamp values were sent to a microcontroller, which performed frequency calculations according to (1) or (3) [3]. Due to the high intensity of calculations for Ω counter, in future work we are going to adapt hardware computational module inside the FPGA device [7]. Such a solution will allow to significantly reduce the number of transferred data, speed up the operation of the module and increase its functionality.

Each channel can be configured separately and work in frequency or time interval (without gating the input circuit) measurement modes. This is especially important for channel 4 that is designed to register 1PPS signal. With a reference to this signal it is possible to determine the timing of the frequency measurements performed in the other channels. According to results obtained in all 4 channels the counter allows to determine vibrations in 4 dimensions (x, y, z and time) and synchronize results with other systems using timing signals from GNSS.

III. Results

In the multidimensional seismometer system it was assumed that the deviation from the nominal frequency of 600 MHz in a 1 ms gate time should be measured with a precision of about 1 Hz or better. We have implemented the described design in a Kintex-7 FPGA device from *AMD Xilinx*, placed on a self-designed test board. The main clock signal of 710 MHz was generated by an external frequency synthesizer driven by a 10 MHz clock signal from the FS725 rubidium standard produced by *Stanford Research System*. Test frequency signals were generated by another FS725 rubidium standard (10 MHz) or the HP8648 signal generator from Agilent (600 MHz or 1 GHz).

Frequency calculations were done outside the chip using either Π or Ω counter principles. In all cases we collected 1000 results and for liner regression calculations we used n=1000 timestamps for each result (Eq. 2). Obtained results are presented in Fig. 2. The Δf value is calculated as the difference of the measured and the average values.

In the case of Π counter, the measurement precision, evaluated as a standard deviation calculated from the sample of of 600 MHz frequency measurements performed at 1 ms time gate, was below 2.5 Hz. After applying the linear

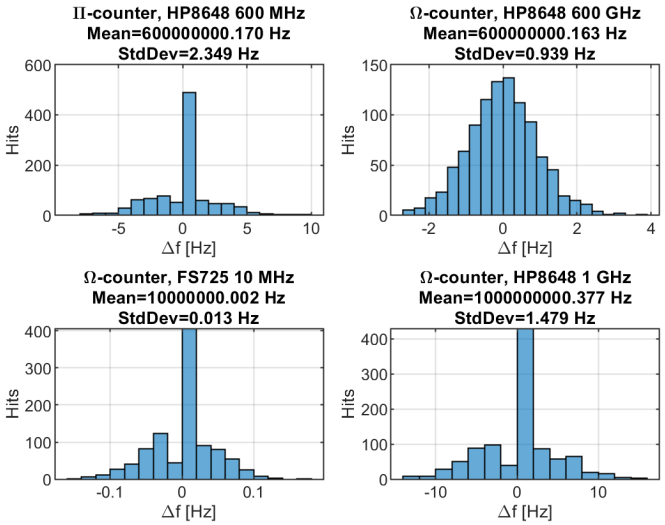

Fig. 2. Example results of frequency measurements at 1 ms gate time.

regression (Ω counter) it was improved about 2.5-fold, to the value below 1 Hz. This meets the requirements for the frequency counter in the seismometric system. Further improvement in precision is possible by extending the measurement gate time.

In addition, under the same conditions, we verified the frequency measurement precision (0.013 Hz) possible to achieve for the 10 MHz signal from the FS725 rubidium standard from *Stanford Research System* (different than the one used for 710 MHz signal generation by the frequency synthesizer) and the maximum frequency at which the integrated frequency counter still operates correctly (1 GHz). Although the result of the direct measurement of the frequency of 1 GHz is correct, it should be noted that such a high frequency is beyond the guaranteed performance of the selected FPGA device (Kintex-7).

IV. Conclusions

The integrated frequency counter meets the requirements set for it in the newly designed seismomteric system, i.e. accurate 600 MHz frequency measurement in 1 ms gate time timestamped and synchronized to 1PPS signal. High performance of the counter was achieved by combining the methods of time stamping, interpolation (both implemented in the FPGA device) and linear regression (calculated outside the counter at this stage). In the next step we are going to implement a hardware computing module of Ω counter inside the FPGA device, connect the counter to the complete seismometric system and check its performance in field conditions.

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